

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.

A DISPOSABLE MOLD RUNNER GATE FOR
SUBSTRATE BASED ELECTRONIC PACKAGES

INS. A1 >

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

This invention relates to encapsulation of substrate based electronic packages using injection molding with a two piece mold and more particularly to the use of a barrier material formed over the gating area of the substrate which is later peeled away and discarded.

(2) DESCRIPTION OF THE RELATED ART

Injection molding using a two piece mold is often used for encapsulation of electronic devices. This requires the formation of a gating area on the substrate surface for removal of the mold runner after the encapsulation is complete and the encapsulant is cured. The gating area usually has a metal formed on the substrate such as palladium or gold. This places severe restrictions on the routing of circuit traces formed on the surface of the

substrate.

U. S. Pat. No. 5,635,671 to Freyman et al.

describes a degating region having a material formed thereon chosen such that the material in the degating region forms a weak bond with the encapsulant used. Freyman et al.

5 describe the used of degating material such as gold so that wiring traces must be routed away from the degating region.

U.S. Pat. No. 5,311,402 to Kobayashi et al.

describes an integrated circuit chip bonded to a circuit board with a cap for hermetically sealing the chip. The cap is bonded to the circuit board at the edges of an open end thereof and bonded to the underside or bottom of the chip.

U.S. Pat. No. 5,099,101 to Millerick et al.

15 describes an automatic laser trimming apparatus for semiconductor integrated chip packages which performs deflashing and degating operations.

U.S. Pat. No. 4,954,308 to Yabe et al. describes a resin encapsulating method using upper and lower half molds.

SUMMARY OF THE INVENTION

Electronic circuit packages typically comprise a substrate with one or more integrated circuit elements attached. Molded packages are often used for the encapsulation of the integrated circuit element because they provide a reliable encapsulation at a reasonable cost.

Fig. 1 shows a cross section view of such a package. The package has a substrate 10 with an integrated circuit element 12 attached to the first surface 26 of the substrate 10. Circuit traces 18 on the first surface 26 of the substrate communicate with circuit traces 22 on the second surface 27 of the substrate using via connections 20 through the substrate. Input/output balls 24 provide ball grid array type input/output connections for the package. The input/output balls can be a material such as solder, solder coated copper, or the like. The connections between the integrated circuit element 12 and the circuit traces 18 on the first surface 26 of the substrate 10 are provided by wire bonds 16.

The substrate based package is encapsulated with a molded encapsulant 14. In most cases the molded encapsulant 14 is a molded plastic. In packages of this type the molded encapsulant is usually formed using an injection molding process using a two piece mold. The two piece mold is

preferred because of cost, but requires a gate region on the substrate as will be explained with reference to Figs. 2-5.

Sub B17

A cross section of a part of a two piece mold is shown in Fig. 2. The mold has an upper part 30, a lower part 28, a cavity 34 in the upper part 30 of the mold and a recess 29 in the lower part 28 of the mold. The substrate 10 with the integrated circuit element 26 attached fits into the recess 29 of the lower part 28 of the mold. As can be seen in Fig. 2, the input/output balls have not been formed on the substrate at this point in the processing. A mold runner channel 32 is formed in the upper part of the mold 30 and forms a path for the uncured encapsulant to flow into the cavity 34 in the upper part 30 of the mold. Fig. 3 is a plan view of the upper part 30 of the mold, taken along line 3-3' of Fig. 2, showing the cavity 34 and the mold runner channel 32.

During the encapsulation process uncured encapsulant is forced to flow from a source, not shown, through the mold runner channel 32 into the cavity 34, thereby filling the cavity. When the encapsulant is cured, encapsulant in the mold runner channel is also cured forming a mold runner 33, as shown in Fig. 4. This mold runner 33 must be removed after the encapsulant has cured. To accomplish the removal of the mold runner 33 a degating

region 36 is typically formed on the first surface 26 of the substrate 10 at the substrate location which will be directly under the mold runner channel 32, see Figs. 2 and 4. The degating region is formed of a material chosen such that the adhesive force between the encapsulant and the degating region material is less than the adhesive force between the encapsulant and the substrate. The degating region material is usually a metal such as gold or palladium.

With degating regions formed in this manner the circuit traces 18 on the first surface of the substrate and vias 20 between the first surface and second surface of the substrate must be routed to avoid the degating region 36, as shown in Fig. 5. The dashed lines in Fig. 5 show the location of the mold runner channel 32 and the perimeter 35 of the cavity. Degating regions of this type consume valuable surface area on the first surface of the substrate which could be used for circuit traces or vias. In addition mold compound material normally will flash outside the degating region and can cause problems.

It is a principle objective of this invention to provide a method of encapsulation of substrate based electronic devices using a gating region on a substrate which can be formed directly over circuit tracing.

It is another principle objective of this invention to provide a substrate, for substrate based electronic devices, wherein the substrate uses a gating region on a substrate which can be formed directly over circuit tracing.

These objectives are achieved by attaching a barrier material to the region of the substrate where the mold runner channel will be located when the package is encapsulated. The barrier material can be attached directly over circuit traces or via holes. The barrier material is chosen such that the adhesive force between the barrier material and the adhesive is less than the adhesive force of the cured encapsulant to the barrier material. After the encapsulation has been completed and the encapsulant cured the mold runner is removed thereby also removing the barrier material.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section view of an encapsulated substrate based electronic package.

5 Fig. 2 shows a cross section view of a two piece mold.

Fig. 3 shows a plan view of the upper part of the two piece mold of Fig. 2 along line 3-3' of Fig. 2.

Fig. 4 shows a cross section view of a prior art encapsulated substrate based electronic package showing a mold runner and gating area.

Fig. 5 shows a top view of a prior art substrate showing a gating area with circuit traces routed away from the gating area.

15 Fig. 6 shows a top view of a substrate of this invention showing a gating area with circuit traces routed in the gating area under the barrier material.

5

Fig. 7 shows a cross section view of a substrate of this invention after the encapsulant has been molded and cured showing barrier material formed in the gating area over the circuit traces and a mold runner over the barrier material. Fig. 7 is a section view of the encapsulated substrate of Fig. 8 taken along line 7-7' of Fig. 8.

15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
339
340
341
342
343
344
345
346
347
348
349
349
350
351
352
353
354
355
356
357
358
359
359
360
361
362
363
364
365
366
367
368
369
369
370
371
372
373
374
375
376
377
378
379
379
380
381
382
383
384
385
386
387
388
389
389
390
391
392
393
394
395
396
397
398
399
399
400
401
402
403
404
405
406
407
408
409
409
410
411
412
413
414
415
416
417
418
419
419
420
421
422
423
424
425
426
427
428
429
429
430
431
432
433
434
435
436
437
438
439
439
440
441
442
443
444
445
446
447
448
449
449
450
451
452
453
454
455
456
457
458
459
459
460
461
462
463
464
465
466
467
468
469
469
470
471
472
473
474
475
476
477
478
479
479
480
481
482
483
484
485
486
487
488
489
489
490
491
492
493
494
495
496
497
498
499
499
500
501
502
503
504
505
506
507
508
509
509
510
511
512
513
514
515
516
517
518
519
519
520
521
522
523
524
525
526
527
528
529
529
530
531
532
533
534
535
536
537
538
539
539
540
541
542
543
544
545
546
547
548
549
549
550
551
552
553
554
555
556
557
558
559
559
560
561
562
563
564
565
566
567
568
569
569
570
571
572
573
574
575
576
577
578
579
579
580
581
582
583
584
585
586
587
588
589
589
590
591
592
593
594
595
596
597
598
599
599
600
601
602
603
604
605
606
607
608
609
609
610
611
612
613
614
615
616
617
618
619
619
620
621
622
623
624
625
626
627
628
629
629
630
631
632
633
634
635
636
637
638
639
639
640
641
642
643
644
645
646
647
648
649
649
650
651
652
653
654
655
656
657
658
659
659
660
661
662
663
664
665
666
667
668
669
669
670
671
672
673
674
675
676
677
678
679
679
680
681
682
683
684
685
686
687
688
689
689
690
691
692
693
694
695
696
697
697
698
699
699
700
701
702
703
704
705
706
707
708
709
709
710
711
712
713
714
715
716
717
718
719
719
720
721
722
723
724
725
726
727
728
729
729
730
731
732
733
734
735
736
737
738
739
739
740
741
742
743
744
745
746
747
748
749
749
750
751
752
753
754
755
756
757
758
759
759
760
761
762
763
764
765
766
767
768
769
769
770
771
772
773
774
775
776
777
778
779
779
780
781
782
783
784
785
786
787
788
789
789
790
791
792
793
794
795
796
797
797
798
799
799
800
801
802
803
804
805
806
807
808
809
809
810
811
812
813
814
815
816
817
818
819
819
820
821
822
823
824
825
826
827
828
829
829
830
831
832
833
834
835
836
837
838
839
839
840
841
842
843
844
845
846
847
848
849
849
850
851
852
853
854
855
856
857
858
859
859
860
861
862
863
864
865
866
867
868
869
869
870
871
872
873
874
875
876
877
878
879
879
880
881
882
883
884
885
886
887
888
889
889
890
891
892
893
894
895
896
897
897
898
899
899
900
901
902
903
904
905
906
907
908
909
909
910
911
912
913
914
915
916
917
918
919
919
920
921
922
923
924
925
926
927
928
929
929
930
931
932
933
934
935
936
937
938
939
939
940
941
942
943
944
945
946
947
948
949
949
950
951
952
953
954
955
956
957
958
959
959
960
961
962
963
964
965
966
967
968
969
969
970
971
972
973
974
975
976
977
978
979
979
980
981
982
983
984
985
986
987
988
989
989
990
991
992
993
994
995
996
997
997
998
999
999
1000

Fig. 10 shows a cross section view of the encapsulated substrate of Fig. 9 taken along line 19-10' of Fig. 9.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refer now to Figs. 1-3 and 6-10 for a description of the preferred embodiments of this invention. Fig. 1 shows a cross section view of a substrate based electronic package. The package has a substrate 10 having a first surface 26 and a second surface 27. The substrate can be a laminate with interior wiring, not shown, and can be ceramic or other material. An integrated circuit element 12 is attached to the first surface 26 of the substrate 10. In this example one integrated circuit element is shown, however a number of integrated circuit elements can be attached to the substrate. Circuit traces 18 on the first surface 26 of the substrate communicate with circuit traces 22 on the second surface 27 of the substrate using via connections 20 through the substrate. In this example wire bonds 16 provide electrical connection between the circuit traces 18 and the integrated circuit element 12.

In this example input/output balls 24 provide ball grid array type input/output connections for the package, however other types of input/output connections can be used. The input/output balls can be formed of conducting material such as copper, solder, solder coated copper, or the like. The package is encapsulated using a molded encapsulant 14 using a method which will now be explained.

5
10
15
20
25

Fig. 6 shows a top surface of a substrate which is to be used as part of the substrate based electronic circuit package. Circuit traces 17 and 18 and the tops of via connections 20 are shown on the surface of the substrate. A barrier material 38 is formed on the surface of the substrate covering the gating area or that part of the substrate which will be under the mold runner channel during the encapsulation step. The dotted lines 41 show the location which will be under the mold runner channel. The barrier material 38 is placed directly over some of the circuit traces 17. The barrier material 38 is a material such as polyimide tape, high temperature plastic, or similar material that is stable at high temperature and has a thickness of between about 0.025 and 0.080 millimeters. The barrier material and the encapsulant are chosen such that the adhesive force between the barrier material and the encapsulant is at least 15 times greater than the adhesive force between the barrier material and the substrate. An integrated circuit element 12 is attached to the surface of the substrate 10 and the integrated circuit element is connected to the circuit traces using wire bonds 16.

The substrate 10 with the integrated circuit element 12 attached to the first surface 26 of the substrate 10 is placed in the two piece mold, shown in Figs. 2 and 3, for encapsulation. The substrate 10 is placed in

the recess 29 formed in the lower part 28 of the mold. The upper part 30 of the mold has a cavity 34 which will mold the shape of the encapsulant. The location of the cavity on the first surface of the substrate is shown by a dashed line 42 in Fig. 6. The uncured encapsulant is injected into the cavity 34 of the upper part 30 of the mold through the mold runner channel 32, see Figs. 2 and 3. The mold runner channel 32 is directly over the gating area 36 of the substrate which has the barrier material 38 formed thereon, see Fig. 6.

Uncured encapsulant is then injected into the cavity 34 in the upper part 30 of the mold, leaving encapsulant in the mold runner channel 32 and cured. The encapsulant can be an encapsulating mold compound material and is cured by time and temperature. As previously indicated encapsulant and the barrier material are chosen such that the adhesive force between the barrier material and the encapsulant is at least 15 times greater than the adhesive force between the barrier material and the substrate. After curing the encapsulant the encapsulated package is removed from the mold. As shown in Fig. 7, the molded encapsulant 14 is formed on the substrate covering the integrated circuit element, not shown in Fig. 7, and leaving a mold runner 33 of encapsulant formed on the barrier material 38.

Fig. 8 shows the top view of the substrate at this point of the processing showing the molded encapsulant 14 and the mold runner 33 formed on the barrier material 38. As can be seen in Figs. 7 and 8 circuit tracings 17 can be 5 routed directly under the barrier material 38 and mold runner 33. Fig. 7 is a cross section view of Fig. 8 taken along line 7-7' of Fig. 8. Since the adhesive force between the barrier material and the encapsulant is greater than the adhesive force between the barrier material and the substrate the mold runner can be broken away from the molded encapsulant 14 thereby peeling away the barrier material as well, as shown in Figs. 9 and 10.

Svb27
Figs. 9 and 10 show the encapsulated package with the mold runner and barrier material removed. Fig. 9 shows the top view of the substrate and Fig. 9 a cross section view taken along line 10-10' of Fig. 9.

The use of the barrier material of this invention makes it possible to form circuit traces in the gating area of the substrate since the circuit traces are protected by 20 the barrier material. The use of the barrier material of this invention also allows the use of any existing substrate material or design that is available. Without the use of barrier material the location of the degating region on the substrate must match the design of the upper part of the

5

mold. The use of the barrier material of this invention avoids the need for a fixed location for a degating region on a substrate for a particular upper mold design and allows the use of different substrate designs without the need to redesign the upper part of the mold.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

TOP SECRET - DTIC